REMARKS

Claims 1-6 are pending in the Application. Claims 1-3 are rejected under 35 U.S.C. § 102(e). Claims 4-6 are rejected under 35 U.S.C. § 103(a). Applicants have cancelled claim 1 without prejudice or disclaimer. Applicants reserve the right to file a continuation application to capture the subject matter of claim 1. Claims 2-4 have been amended. Claims 16-19 have been added and hence claims 1-6 and 16-19 are pending. Applicants respectfully traverse the rejections for at least the reasons stated below and respectfully request that the Examiner reconsider and withdraw all outstanding rejections.

I. REJECTIONS UNDER 35 U.S.C. § 102(e):

The Office Action has rejected claims 1-3 under 35 U.S.C. § 102(e) as being anticipated by *Lien* (U.S. Patent No. 6,338,993). Applicants respectfully traverse the rejections for at least the reasons stated below and respectfully request that the Examiner reconsider and withdraw all outstanding rejections.

For a claim to be anticipated under 35 U.S.C. § 102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. § 2131.

Lien does not disclose "*a plurality of core spacers, each of the plurality of core spacers residing along an edge of the plurality of core gate stacks*" as recited in claim 2. The Examiner directs Applicants' attention to element number 400 in FIGURE 7 as disclosed in the above-cited claim limitation. Paper No. 6, page 3. Instead, *Lien* states:

> Next, referring to FIG. 3, a *silicon nitride layer 400 is blanket deposited over the memory cell region 30, the NMOS region 20 and the PMOS region 10 and atop the gate structures on these regions.* The *silicon nitride layer 400 is used as a protective layer of the memory cell region 30 in a following salicide process.* In a preferred embodiment of the present invention, the silicon nitride layer 400 has a thickness about from 500 to 1500 angstroms. Column 3, lines 56-63.

Thus, *Lien* discloses using a silicon nitride layer 400 as a protective layer. Spacers are used to isolate gate and source and drain contacts. However, silicon nitride layer 400 as disclosed in *Lien* is not used to isolate gate and source and drain contact, but instead is used as a protective layer of the memory cell region in a following salicide process. Therefore, *Lien* does not disclose all the limitations of claim 2, and thus *Lien* does not anticipate claim 2. M.P.E.P. § 2131.

Lien also does not disclose "a *polysilicon capping layer above said WSi layer* and an *additional capping layer above said polysilicon capping layer*" as recited in claim 16. Instead, *Lien* states:

> Furthermore, a *doped polysilicon gate 240 is formed on the gate oxide layer 220 on the memory cell region 30 and a tungsten silicide (Wsi_x) layer 250* is formed on the doped polysilicon gate 240. Subsequently, a *cap layer 260 formed of TEOS material or silicon nitride material is formed on the tungsten silicide layer 250.* The stack structure consisting of the layer 220, 240, 250 and 260 is the gate structure of the memory cells. Column 3, lines 43-50.

Thus, *Lien* discloses a polysilicon gate formed on the gate oxide layer on a memory cell region and a tungsten silicide layer formed on the doped polysilicon gate. *Lien* further teaches a cap layer of TEOS material or silicon nitride material formed on the tungsten silicide layer. However, *Lien* does not disclose a *layer of polysilicon above the WSi layer*. Further, *Lien* does not disclose an *additional capping layer above a polysilicon capping layer*. Therefore, *Lien* does not disclose all the limitations of claim 6, and thus *Lien* does not anticipate claim 6. M.P.E.P. § 2131.

For at least the above reasons, claims 2 and 6 are not anticipated by *Lien*. Claims 3 and 17-19 each recite combinations of features including the above limitations, and thus are not anticipated for at least the above reasons. Claims 3 and 17-19 recite additional features, which, in combination with the features of the claims upon which they depend, are not anticipated by *Lien*.

For example, *Lien* does not disclose "wherein said *additional capping layer functions as an antireflective layer*" as recited in claim 17. As stated above, *Lien* does not disclose an additional capping layer. Hence, *Lien* does not disclose an additional capping layer functioning as an antireflective layer. Therefore, *Lien* does

not disclose all the limitations of claim 17, and thus *Lien* does not anticipate claim 17. M.P.E.P. § 2131.

Lien also does not disclose "wherein said *additional capping layer is a SiN layer*" as recited in claim 18. As stated above, *Lien* does not disclose an additional capping layer. Hence, *Lien* does not disclose an additional capping layer that is a SiN layer. Therefore, *Lien* does not disclose all the limitations of claim 18, and thus *Lien* does not anticipate claim 18. M.P.E.P. § 2131.

Lien also does not disclose "wherein said *additional capping layer is a SiON layer*" as recited in claim 19. As stated above, *Lien* does not disclose an additional capping layer. Hence, *Lien* does not disclose an additional capping layer that is a SiON layer. Therefore, *Lien* does not disclose all the limitations of claim 19, and thus *Lien* does not anticipate claim 19. M.P.E.P. § 2131.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found with *Lien*, and thus claims 2-3 and 16-19 are not anticipated by *Lien*.

It is noted that words are italicized only for emphasis. Words that are italicized are not meant to imply that these are the only limitations not disclosed in the cited prior art.

II. REJECTIONS UNDER 35 U.S.C. § 103:

The Office Action has rejected claims 4-6 as being unpatentable over *Lien* in view of *Yang* (U.S. Patent No. 5,977,601). Applicants respectfully traverse these rejections for at least the reasons provided below and respectfully request that the Examiner reconsider withdrawing these rejections.

A. The Examiner has not provided a *prima facie* case of obviousness for rejecting claims 4-6.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to

make the claimed inventions. M.P.E.P. § 2142. The motivation or suggestion to combine references must come from one of three possible sources: the nature of the problem to be solved, the teaching of the prior art and the knowledge of persons of ordinary skill in the art. *In re Route*, 47 U.S.P.Q.2d. 1453,1458 (Fed. Cir. 1998). The showings must be clear and particular. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 200); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

In order to reject under 35 U.S.C. 103, therefore, the Examiner must provide a proper motivation for combining or modifying the references. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457-1458 (Fed. Cir. 1998); M.P.E.P. § 2142. The Examiner's motivation for modifying *Lien* to have a layer of polysilicon above the WSi layer and a capping layer above the layer of polysilicon is "to improve the density of the core of gate stacks." Paper No. 6, page 5.

The Examiner has not established a *prima facie* case of obviousness for combining *Lien* with *Yang*, as there is no suggestion or motivation in either *Lien* or *Yang*, or in their combination, or in the knowledge of those ordinarily skilled in the art, to combine the teaching of protecting the memory cells in the embedded DRAM by a protective layer during a salicide process, as taught in *Lien*, with the teaching of increasing the density of a memory gate structure in a deep submicron memory core using conventional DUV lithography techniques, as taught in *Yang*. *Lien* states:

> The present invention discloses a method to fabricate embedded DRAM with salicide logic cells and memory cells. A substrate is provided and isolation regions are formed thereon to define a logic cell region and a memory cell region. Besides, a gate structure is formed on the memory cell region. Light-doped-drain (LDD) regions of the logic cells are formed in the substrate adjacent to the gate structure. A silicon nitride layer is formed on the substrate and the gate structure. The silicon nitride layer is etched to expose the substrate in the logic cell region. An ion implantation process is performed to form source/drain regions of the logic cell region. Finally, *a salicide process is performed to form a salicide layer on the source/drain regions of the logic cell region, wherein the gate structure of the*

> *memory cell region is protected by the silicon nitride layer during the salicide process*. Column 2, lines 8-22.

Thus, *Lien* teaches performing a salicide process to form a salicide layer on the source/drain regions of the logic cell region where the gate structure of the memory cell region is protected by the silicon nitride layer during the salicide process.

Yang states:

> A memory gate stack in a *high density memory core has spaces on the order of less than 0.25 microns using conventional deep ultraviolet (DUV) lithography techniques by depositing a layer of silicon oxynitride over a plurality of layers, and a thin resist layer overlying on the silicon oxynitride layer.* The resist layer has a thickness sufficient to withstand removal during etching of the silicon oxynitride layer, for example about 3,000 Angstroms to about 4,000 Angstroms. The silicon oxynitride layer has a sacrificial portion having a thickness at least about 500 Angstroms, and a stop-layer thickness, used for spacer formation following etching of the memory gate, of at least 1,000 Angstroms. The use of silicon oxynitride as an antireflective coating layer in combination with the thin resist optimizes the resolution of DUV lithography, enabling formation of spacers having widths less than about 0.24 microns. In addition, the sacrificial layer of the silicon oxynitride layer enables self-aligned etching of the plurality of layers to form the memory gate stack, while maintaining sufficient thickness for spacer formation. Abstract.

Thus, *Yang* teaches a memory gate stack that has spaces on the order of less than 0.25 microns using conventional deep ultraviolet (DUV) lithography techniques by depositing a layer of silicon oxynitride over a plurality of layers and a thin resist layer overlying on the silicon oxynitride layer.

The Examiner has not shown from either the nature of the problem to be solved, the teaching in the prior art or the knowledge of persons of ordinary skill in the art why one skilled in the art would combine the teaching of performing a salicide process to form a salicide layer on the source/drain regions of the logic cell region, where the gate structure of the memory cell region is protected by the silicon nitride layer during the salicide process, with the teaching of increasing the density of the memory gate structure in a deep submicron memory core using conventional DUV lithography techniques. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

The Examiner must provide **objective evidence** for combining *Lien*, which teaches performing a salicide process to form a salicide layer on the source/drain regions of the logic cell region where the gate structure or the memory cell region is protected by the silicon nitride layer during the salicide process, with *Yang*, which teaches increasing the density of a memory gate structure in a deep submicron memory core using conventional DUV lithography techniques. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

As stated above, the Examiner's motivation for modifying *Lien* to have a layer of polysilicon above the WSi layer and a capping layer above the polysilicon layer is to improve the density in a core of gate stacks. The Examiner does not show why *Lien* should be modified to have a layer of polysilicon above the WSi layer and a capping layer above a polysilicon layer, from either the nature of the problem to be solved, the teaching in the prior art or the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). Further, the Examiner has not shown why *Lien* should be modified to improve the density in a core of gate stacks, from either the nature of the problem to be solved, the teaching in the prior art or the knowledge of persons of ordinary skill in the art. *Id.*

Further, the Examiner must submit **objective evidence** and not rely on his own subjective opinion in support of modifying *Lien* to have a layer of polysilicon above the WSi layer and a capping layer above the polysilicon layer. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Further, the Examiner must submit **objective evidence** and not rely on his own subjective opinion in support of modifying *Lien* to improve the density of the core gate stacks. *Id.* Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 4-6.

Furthermore, if the proposed modification or combination of the prior art would *change the principle of the operation of the prior art invention being modified*, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959). Further, if the proposed modification would *render the prior art invention being modified*

unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). *Lien* states:

> Therefore, *a method for fabricating an embedded DRAM on a substrate is needed and the memory cells of the embedded DRAM must be protected by a protective layer during the salicide process of the logic cells in the device.* Column 2, lines 1-4.

Lien further states:

> Furthermore, a *doped polysilicon gate 240 is formed on the gate oxide layer 220 on the memory cell region 30 and a tungsten silicide (Wsi_x) layer 250 is formed on the doped polysilicon gate 240.* Subsequently, a cap *layer 260 formed of TEOS material or silicon nitride material is formed on the tungsten silicide layer 250.* The stack structure consisting of the layer 220, 240, 250 and 260 is the gate structure of the memory cells. Column 3, lines 43-50.

Lien further states:

> Next, referring to FIG. 3, a *silicon nitride layer 400 is blanket deposited over the memory cell region* 30, the NMOS region 20 and the PMOS region 10 and atop the gate structures on these regions. *The silicon nitride layer 400 is used as a protective layer of the memory cell region 30 in a following salicide process.* In a preferred embodiment of the present invention, the silicon nitride layer 400 has a thickness about from 500 to 1500 angstroms. Column 3, lines 56-63.

Thus, *Lien* teaches a doped polysilicon gate formed on a gate oxide layer of the memory cell region and a tungsten silicide layer formed on the doped polysilicon gate. *Lien* further teaches a cap layer formed on the tungsten silicide layer. *Lien* further teaches that the memory cells of the embedded DRAM are protected by a silicon nitride layer during the salicide process of the logic cells in the device.

Yang states:

> FIGS. 2A, 2B and 2C summarize a method of etching a semiconductor wafer for formation of a memory gate stack 60 according to an embodiment of the present invention. As shown in FIG. 2A a plurality of layers 80 are first formed overlying the substrate 12. *The layers 60 include a tunnel oxide layer 15 overlying on the silicon substrate 12, a first polysilicon layer 62 overlying on the tunnel oxide layer 15, and an oxide-nitride-oxide (ONO) layer 64 overlying on the first*

> *polysilicon layer 62. The stack 60 also includes a second polysilicon layer 66 overlying on the ONO layer 64, a silicide (Wsi_x) layer overlying on the second polysilicon layer 66, a polysilicon cap layer 70 overlying on the silicide layer 68, and a silicon oxynitride (SiON) layer 72 overlying on the polysilicon cap layer 70.* The silicon oxynitride layer 72 serves as an antireflective coding (ARC) layer, and hence may be used for many reduced-size critical dimension semiconductor devices. Both the polysilicon cap layer 70 and the silicon oxynitride layer 72 are deposited using conventional chemical vapor deposition (CVD) or plasma enhanced chemical vapor deposition (PECVD) techniques. The polysilicon cap layer 70 typically includes undoped polysilicon and has a thickness of about 500 Angstroms. The silicon oxynitride layer includes silicon oxynitride (e.g., SiO_x, N_y (wherein x and y represent the atomic percentage of oxygen and nitrogen, respectively) and has a thickness of about 400 Angstroms. Column 4, lines 10-36.

Thus, *Yang* teaches a plurality of layers formed overlying the substrate where the plurality of layers include a first polysilicon layer 62 and an oxide-nitride-oxide (ONO) layer 64 overlying on the first polysilicon layer 62. The plurality of layers further includes a second ploysilicon layer 66 overlying on the ONO layer 64. The plurality of layers further includes a silicide layer 68 overlying on the second polysilicon layer 66. The plurality of layers further includes a polysilicon cap layer 70 overlying on the silicide layer 68. The plurality of layers further includes the silicon oxynitride (SiON) layer 72 overlying on the polysilicon cap layer 70.

Hence, by combining *Lien* and *Yang*, *Lien* would not be able to form the gate structure of the memory cells consisting of the layers of a doped polysilicon gate, a tungsten silicide layer formed on the doped polysilicon gate, and a cap layer formed on the tungsten silicide layer. Instead, *Lien* would have to be modified to have the gate structure of the memory cells include the layers of a silicon oxynitride layer overlying a polysilicon layer overlying a silicide layer overlying a second polysilicon layer overlying an ONO layer overlying a first polysilicon layer. By including these additional layers in the memory cell region in *Lien*, *Lien* **would not be able to protect the gate structure of the memory cell region by the silicon nitride layer during the salicide process since the silicon nitride layer would not exist**. That is, by combining *Lien* with *Yang*, the *principle of operation in Lien would change* and subsequently *render the operation of Lien to perform its purpose unsatisfactory.*

Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 4-6.

B. *Lien* and *Yang*, taken singly or in combination, do not teach or suggest the following limitations.

Lien and *Yang*, taken singly or in combination, do not teach or suggest "*a layer of polysilicon above the WSi layer and a capping layer above the polysilicon layer*" as recited in claim 4 and similarly in claim 16. The Examiner directs Applicants' attention to layer 700 in *Lien* as teaching the polysilicon layer above the WSi layer. Paper No. 6, page 5. The Examiner further directs Applicants' attention to Figure 5, column 5, lines 23-26 and column 5, lines 39-46 of *Yang* as teaching a capping layer above the polysilicon layer. Paper No. 6, page 5. Instead, *Lien* states:

> Note also that in FIG. 7, a polysilicon layer (2500-5000 angstroms) is blanket deposited over the interlayer dielectric layer 600 and the polysilicon layer is then etched back or by using CMP *to form a polysilicon plug 700*. Column 4, lines 51-55.

Thus, *Lien* teaches forming a polysilicon plug 700. A person of ordinary skill in the art would not interpret a polysilicon plug as teaching or suggesting a polysilicon layer above a WSi layer. Applicants respectfully direct the Examiner's attention to Figure 7 which shows that polysilicon plug 700 lies in between the gate structures and the memory cell region and not above the WSi layer. Further, *Yang* states:

> FIGS. 2A, 2B and 2C summarize a method of etching a semiconductor wafer for formation of a memory gate stack 60 according to an embodiment of the present invention. As shown in FIG. 2A a plurality of layers 80 are first formed overlying the substrate 12. The layers 60 include a tunnel oxide layer 15 overlying on the silicon substrate 12, a first polysilicon layer 62 overlying on the tunnel oxide layer 15, and an oxide-nitride-oxide (ONO) layer 64 overlying on the first polysilicon layer 62. The stack 60 also includes a second polysilicon layer 66 overlying on the ONO layer 64, a silicide (WSi_x) layer overlying on the second polysilicon layer 66, *a polysilicon cap layer 70 overlying on the silicide layer 68*, and a silicon oxynitride (SiON) layer 72 overlying on the polysilicon cap layer 70. The silicon oxynitride layer 72 serves as an antireflective coding (ARC) layer, and hence may be used for many reduced-size critical dimension semiconductor devices. Both the polysilicon cap layer 70 and the silicon oxynitride layer 72

> are deposited using conventional chemical vapor deposition (CVD) or plasma enhanced chemical vapor deposition (PECVD) techniques. The polysilicon cap layer 70 typically includes undoped polysilicon and has a thickness of about 500 Angstroms. The silicon oxynitride layer includes silicon oxynitride (e.g., SiO_x, N_y (wherein x and y represent the atomic percentage of oxygen and nitrogen, respectively) and has a thickness of about 400 Angstroms. Column 4, lines 10-36.

Thus, *Yang* teaches a polysilicon cap layer 70 overlying on the silicide layer 68. *Yang* does not teach a capping layer above the polysilicon layer. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 4 and 16. M.P.E.P. §2143.

Lien and *Yang*, taken singly or in combination, do not teach or suggest "*wherein the capping layer is a SiN layer*" as recited in claim 5 and similarly in claim 18. The Examiner directs Applicants' attention to column 4, line 34 of *Yang* as teaching the above-cited claim limitation. Paper No. 6, page 5. Instead, *Yang* states:

> The silicon oxynitride layer includes silicon oxynitride (e.g., SiO_x, N_y (wherein x and y represent the atomic percentage of oxygen and nitrogen, respectively) and has a thickness of about 400 Angstroms. Column 4, lines 32-36.

Thus, *Yang* teaches a silicon oxynitride layer 32 overlying a polysilicon cap layer 70. Applicants are confused as to whether the Examiner directs Applicants' attention to polysilicon cap layer 70 or silicon oxynitride layer 72 as teaching the capping layer referred to in claim 4. Applicants respectfully request the Examiner to clarify whether the Examiner interprets polysilicon cap layer 70 or silicon oxynitride layer 72 as teaching the capping layer referred to in claim 4, pursuant to 37 C.F.R. §1.104(c)(2). In either case, neither layer teaches a SiN layer. As indicated above, *Yang* simply teaches a polysilicon cap layer 70 that typically includes undoped polysilicon. *Yang* further teaches a silicon oxynitride layer 72 that includes silicon oxynitride and not simply silicon nitride. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 5 and 18. M.P.E.P. §2143.

C. **Conclusion Regarding 35 U.S.C. § 103 Rejections.**

As a result of the foregoing, Applicants respectfully assert that since there are numerous claim limitations not taught or suggested in the cited prior art, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 4-6 and 17-19 in view of the cited prior art.

It is noted that words are italicized only for emphasis. Words that are italicized are not meant to imply that these are the only limitations not taught or suggested in the cited prior art.

III. CONCLUSION

As a result of the foregoing, it is asserted by Applicants that claims 1-6 and 16-19 in the Application are in condition for allowance, and Applicants respectfully request an early allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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